REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-3, 8-10, 14, 24, 30, and 34 are presently active in this case, Claim 1 having been amended by the present amendment, and Claims 4-7, 11-13. 15-23, 25-29 and 31-33 having been canceled.

In the outstanding Official Action, Claims 1-3, 8-10, 14, 24, 30, and 32-34 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement; and Claims 1-3, 8-10, 14, 24, 30, and 32-34 were rejected under 30 U.S.C. 103(a) as being unpatentable over US Patent 6,275,239 to Ezer.

In response to the rejection of Claims 1-3, 8-10, 14, 24, 30, and 32-34 under 35 U.S.C. 112, first paragraph, Claim 1 has been amended consistent with the disclosure, for example, at page 18, lines 24 to 27, and page 21, lines 10 to 13 of Applicants' specification. Accordingly, no new matter has been added, and the outstanding rejection based on 35 U.S.C. 112, first paragraph, is believed to have been overcome.

In view of the clarification provided by the changes to amended Claim 1, it is respectfully submitted that the rejection of Claims 1-3, 8-10, 14, 24, 30, and 32-34 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6275239 to Ezer has also been overcome, as next discussed.

Ezer discloses a media coprocessor in which a small amount of resident dispatcher code 701 in the MSP Instruction Memory 702 reads code for the next function to be performed from a task list updated by the CPU (see column 10, lines 21-24), and the MSP then initiates a DMA transfer of the task code into Instruction Memory 702. Further, Ezer discloses that the task initiates DMA transfers of input data buffers from DRAM 707 to Data

Memory 708 (column 10, lines 25-29). In other words, according to Ezer, a dispatcher transfers a task code for the next function to Instruction memory, and the task performs DMA transfer.

In contrast, amended Claim 1 recites that the control processor makes reservation of sending an instruction to the DMA controller so that the data and instruction group required for the next processing is prepared in advance while continuing the processing which is currently being performed. According to the claimed invention, when an instruction is sent to the DMA controller in advance at the time of the bit stream decoding which is processing at the stage prior to the noiseless decoding, the delay is concealed, and the general purpose processor 10 can continue operation during the two processings with the result that wasted time is eliminated and processing speed is improved. Further, the arithmetic processing of audio data by VLIW with the coprocessor and DMA control processing with the general purpose processor can be executed in parallel, and thus the operation required for DMA control can be concealed.

It is respectfully submitted that Ezer fails to teach reservation of sending an instruction to the DMA controller so that the data and instruction group required for the next processing is prepared in advance while continuing the processing which is currently performed. In other words, Ewer does not teach to reserve sending of an instruction to the DMA controller while continuing the currently executing processing. Accordingly, in view of this deficiency, it is respectfully submitted that Claim 1 and the remaining claims dependent therefrom patentably define over Ewer and the outstanding rejection on the merits has also been overcome. Withdrawal thereof is therefore also respectfully requested.

Consequently, in view of the present amendment and in light of the above comments, no further issues are believed to be outstanding, and the present application is believed to be

in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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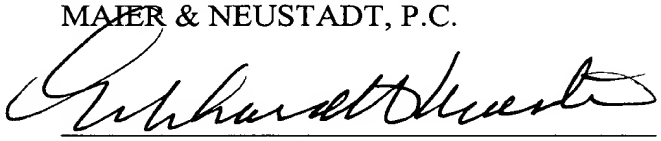

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